

In accordance with the guidelines and waived provisions of 37 C.F.R. 1.121 promulgated in the USPTO announcement of January 31, 2003, please make the following amendments.

IN THE CLAIMS:

Please amend the claims as follows.

1. (Currently Amended) A semiconductor device comprising:
an epitaxial semiconductor substrate having an expitaxial region formed by epitaxial growing silicon on a silicon substrate using Cz method of silicon included in at least an upper portion thereof; and
a diffusion layer formed in said expitaxial region, by using a dopant ion having a relatively large mass number,
wherein said diffusion layer is formed shallower than said epitaxial region.
2. (Original) The semiconductor device of Claim 1, wherein said epitaxial region has a <110>-oriented zone axis.
3. (Previously Amended) The semiconductor device of Claim 1, wherein said diffusion layer is formed by using, as said dopant ion, an indium ion.
4. (Previously Amended) The semiconductor device of Claim 1, wherein said diffusion layer corresponds to a pocket diffusion layer of a MIS semiconductor device, and said MIS semiconductor device includes:
a gate electrode formed above said epitaxial region with a gate insulating film sandwiched therebetween;
a source/drain diffusion layer of a first conductivity type formed in a source/drain region of said epitaxial region at a distance from a region below a side face of said gate electrode;

an extension diffusion layer of the first conductivity type formed in said epitaxial region between said source/drain diffusion layer and said region below the side face of said gate electrode and having shallower junction than said source/drain diffusion layer; and

said pocket diffusion layer of a second conductivity type formed in said epitaxial region under said extension layer.

5. (Previously Amended) The semiconductor device of Claim 4, wherein said extension diffusion layer is formed by using an antimony ion as a dopant.

6. (Previously Amended) A semiconductor device comprising:
a semiconductor substrate composed of silicon and having a main surface of {110}-orientation; and

a diffusion layer formed, by using a dopant ion having a relatively large mass number, in said semiconductor substrate.

7. (Previously Amended) The semiconductor device of Claim 6, wherein said diffusion layer is formed by using, as said dopant ion, an indium ion.

8. (Previously Amended) The semiconductor device of Claim 6, wherein said diffusion layer corresponds to a pocket diffusion layer of a MIS semiconductor device, and said MIS semiconductor device includes:

a gate electrode formed above said semiconductor substrate with a gate insulating film sandwiched therebetween;

a source/drain diffusion layer of a first conductivity type formed in a source/drain region of said semiconductor substrate at a distance from a region below a side face of said gate electrode;

an extension diffusion layer of the first conductivity type formed in said semiconductor substrate between said source/drain diffusion layer and said region

below the side face of said gate electrode and having shallower junction than said source/drain diffusion layer; and

said pocket diffusion layer of a second conductivity type formed in said semiconductor substrate under said extension diffusion layer.

9. (Amended) The semiconductor substrate of Claim 8, wherein said extension diffusion is formed by using an antimony ion as a dopant.

10.-27. (Withdrawn)

28. (Previously Added) The semiconductor device of Claim 3, wherein said diffusion layer is formed by said indium ion at a dose of $5 \times 10^{13}/\text{cm}^2$ or more.

29. (Previously Added) The semiconductor device of Claim 2, wherein said diffusion layer is formed by using, as said dopant ion, an indium ion.

30. (Previously Added) The semiconductor device of Claim 3, wherein said diffusion layer corresponds to a pocket diffusion layer of a MIS semiconductor device, and said MIS semiconductor device includes:

a gate electrode formed above said epitaxial region with a gate insulating film sandwiched therebetween;

a source/drain diffusion layer of a first conductivity type formed in a source/drain region of said epitaxial region at a distance from a region below a side face of said gate electrode;

an extension diffusion layer of the first conductivity type formed in said epitaxial region between said source/drain diffusion layer and said region below the side face of said gate electrode and having shallower junction than said source/drain diffusion layer; and

Application No.: 09/865,546
Attorney Docket No.: 740819-560
Art Unit 2829
Page 5

said pocket diffusion layer of a second conductivity type formed in said epitaxial region under said extension diffusion layer.

31. (Previously Added) The semiconductor device of Claim 30, wherein said extension diffusion layer is formed using an antimony ion as a dopant.

32. (Canceled)

33. (Previously Added) The semiconductor device of Claim 3, wherein said epitaxial semiconductor substrate has a laminated structure including a substrate composed of silicon, and said epitaxial region formed on said substrate by epitaxial growth of silicon.

34. (Previously Added) The semiconductor device of Claim 1, wherein said diffusion layer is formed by using, as said dopant ion, an antimony ion.

35. (Previously Added) The semiconductor device of Claim 7, wherein said diffusion layer is formed by said indium ion at a dose of $5 \times 10^{13}/\text{cm}^2$ or more.

36. (Previously Added) The semiconductor device of Claim 7, wherein said diffusion layer corresponds to a pocket diffusion layer of a MIS semiconductor device, and said MIS semiconductor device includes:

a gate electrode formed above said semiconductor substrate with a gate insulating film sandwiched therebetween;

a source/drain diffusion layer of a first conductivity type formed in a source/drain region of said semiconductor substrate at a distance from a region below a side face of said gate electrode;

an extension diffusion layer of the first conductivity type formed in said semiconductor substrate between said source/drain diffusion layer and said region

Application No.: 09/865,546
Attorney Docket No.: 740819-560
Art Unit 2829
Page 6

Cancel

below the side face of said gate electrode and having shallower junction than said source/drain diffusion layer; and

said pocket diffusion layer of a second conductivity type formed in said semiconductor substrate under said extension diffusion layer.

37. (Previously Added) The semiconductor device of Claim 36, wherein said extension diffusion layer is formed using an antimony ion as a dopant.

38. (Previously Added) The semiconductor device of Claim 6, wherein said diffusion layer is formed by using, as said dopant ion, an antimony ion.
